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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/409,940	09/30/1999	BRYAN KEITH BULLIS	RAL9-99-0056	6159

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SAWYER LAW GROUP LLP
PO BOX 51418
PALO ALTO, CA 94303

EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/409,940	BULLIS ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 21 March 2005 has been entered.

Response to Arguments

2. Applicant's arguments filed 21 March 2005 have been fully considered.

Regarding applicant's response to 103(a) rejection: The examiner first notes that, as acknowledged by applicants, the Board of Patent Appeals affirmed the examiners 35 USC 103(a) rejection of previously presented independent claims 1, 10, and 17. Applicants have now amended independent claims 1, 10, and 17 to recite the limitation "wherein the checker further "calculates" the desired output", instead of "wherein the checker further "determines" the desired output" as previously presented. The examiner submits that this single word amendment does not render the claimed subject matter non-obvious over the prior art for the following reasons. First, the examiner notes that the specification does not specifically address how the claimed checker 'calculates" the

desired output. The examiner has therefor interpreted the claim using the plan meaning of the term "calculate", i.e. to ascertain by computation. This feature is rendered obvious by Hollander because Hollander teaches that checking can be done by "comparing results", or as "computed by a predictor simulator". (CL1-L53-55) Second, applicant's arguments relating to certain features such as the generator being replaced by another island during integration, and the test case providing only data and request for service, as recited in the specification one page 13, lines 7-20 are not persuasive since these features are not specifically recited in the language of the claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In this case, applicant's arguments appear to be more specific than the claims require. (However, applicants can always amend the claims to include any such features that are believed to clearly distinguish the claimed invention over the prior art.) Third, applicants appear to be engaging in piecemeal analysis by arguing that, for example, Guruswamy does not teach the use of a checker to check outputs of the island, or sufficient intelligence in the generator. Guruswamy teaches cell layout generation including islands while Hollander teaches a test generator and checker. The claimed limitations are therefor rendered obvious by the combination of Hollander and Guruswamy as cited below under 103(a) rejections. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

It is also noted that applicant's arguments relating to synchronizing the checker with the test generation module are not persuasive since Hollander clearly teaches that the test generator module and the checker can constantly synchronize" (col. 8, lines 28-30), which teaches synchronization of dynamic inputs with checking of expected responses to those inputs. This issue was addressed (and affirmed) by the Board of Patent Appeals decision rendered on 29 October 2004 (See: page 13, line 12).

The examiner therefor maintains the rejection of claims 1-23 as obvious in view of the combination of Hollander and Guruswamy using reasoning set forth above and below under 103(a) rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. ***Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,182,258 issued to Hollander in view of U.S. Patent 6,006,024 issued to Guruswamy et al.***

*Independent claim 1 is drawn to a system for providing **simulation** of an **integrated circuit** consisting of:*
*A **snooper** coupled with **the interface** monitoring island **output**.*
*A **checker** coupled with **the interface** for checking whether output is **desired output**.*
*A **generator** coupled with **the island** for providing an **input** to the island.*
*A **test case** directing generator to **calculate** output based on input, intelligence to provide input based on request, generator performs particular simulation.*

*Regarding independent claims 1, 10, and 17: Hollander teaches a system, method, and computer code for functionally verifying an integrated circuit design that monitors (i.e. **snoops**) the **simulation** of an **integrated circuit** design via a **checker** (with an **interface**) and including a **test generator** **using a** **test case** **which includes automation** (i.e. **intelligence** for directing test) for determining the defective behavior (for **desired output**) of the circuit in a semiconductor. (Abstract, Summary of Invention, CL3-L37, CL4-L66-CL5-L7, CL8-L30, CL10-L21, Figs. 1-5)*

In the abstract Hollander recites:
"The invention is platform and simulator-independent, and is adapted for integration with Verilog, VHDL, and C functions. A modular system environment ensures interaction with any simulator through a unified **system interface** that supports multiple external types. A **test generator** module automatically creates **verification tests** from a functional description. A test suite can include any **combination of statically and dynamically-generated tests.** Directed generation constrains generated tests to specific functionalities. Test parameters are varied at any point during generation and random stability is supported. A **checking module** can perform any combination of static and dynamic checks."

*Hollander does not explicitly teach verification (testing) a substrate incorporating cells via an **island**.*

*Guruswamy teaches a **cell layout generation** system environment that includes **islands** for an integrated circuit design. (Abstract, Detailed Description, CL9-L29, CL50-L30-65, Figs. 1-5, 60-67)*

*It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teaching of Hollander relating to a system for functionally verifying an integrated circuit design that monitors (**snoops**) the **simulation** of an **integrated circuit** design via a **checker** and including a **test generator** **using a test case**, with the teachings of Guruswamy relating to a **cell layout generation** system environment that includes **islands** for an integrated circuit design to realize the claimed method for self-checking in an ASIC design. From a motivational standpoint, it further would have been obvious to apply the well known integrated circuit hardware verification techniques (i.e. "monitor (snooper)", "generator", "interface, and "checker") as taught by Hollander and simply include an **interface** to the **island** of an ASIC design to provide test case input and output data during simulation.*

*Regarding dependent claims 2-9, 11-16, 18-23: Hollander teaches a system where the **checker** incorporates and **interface** (**coupled**) to monitor (i.e. **snooper**) and **automatic test generator** for use in **integrated circuit** design where the generator and checker are obviously **reusable**. Hollander also teaches that the use a **test case** in monitoring the operation of an integrated circuit simulation. (Abstract, Summary of Invention, CL3-L37, CL4-L66-CL5-L7, CL8-L30, CL10-L21, Figs. 1-5)*

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"A Model for SIMOX Buried-Oxide High-Field Conduction", Krska et al, IEEE Transactions on Electron Devices, Vol. 43, No. 11, November 1996 teaches substrate simulation including an interface to a substrate island.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: 571-273-8300

Fred Ferris, Patent Examiner
Simulation and Emulation, Art Unit 2128
U.S. Patent and Trademark Office
Randolph Building, Room 5D19
401 Dulany Street
Alexandria, VA 22313
Phone: (571-272-3778)
Fred.Ferris@uspto.gov
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